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SPERRY RAND

UNIVAC 9400 SYSTEM

Program Description Drawing

CUSTOMER ENGINEERING

SPERRY RAND UNIVAC

DRAWING NO. 4091651

REVISION D

CUSTOMER ENGINEERING
PRODUCT DIAGNOSTIC SOFTWARE

9400 - 5017 Tape Control Unit Test

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REVISION STATISTICS RECORD

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-	D	7/1/69	R. C. Meltzer	A89794	A30190023
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REVISION DESCRIPTION RECORD

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REV	DESCRIPTION
-	Release
A	1108 to 9400 Assembler Conversion. Modify to allow for pre-parameterization.
B	Corrected per RFC #54331 and RFC #52913.
C	Amend Program Description Drawing in accordance with RFC 46785
D	Enhance program performance

Table of Contents

1. INTRODUCTION

1.1 Purpose - This document describes the 9400 Maintenance and Acceptance Routine (MAR) for the Uniservo XII/XVI Magnetic Tape Subsystem Control Unit.

1.2 Major Objectives - The objective of this MAR is to perform a functional test of the Uniservo XII/XVI Control Unit. Test organization and operator options are intended to satisfy the needs of Design, Quality Control, and Field Engineering personnel in checkout, acceptance, and maintenance activities.

1.3 Equipment Configurations - All equipment configurations must be connected to the Selector (SLR) I/O Channels of the 9400 Processor. When the Dual Access and the Simultaneity hardware options are present, the two channel/control unit interfaces must be on opposite Selector Channels. However, for the purposes of this program they must have identical subchannel numbers. The program will operate the following equipment configuration.

- XII/XVI Control/Handler 9-Track Type 5017-00, 01
- XII Master Unit 9-Track Type 0861-00, 02
- XII Slave Unit 9-Track Type 0861-01, 03
- XII Master Unit 7-Track Type 0861-04, 06
- XII Slave Unit 7-Track Type 0861-05, 07
- W/R, R/R Simultaneity Feature 1600 bpi Phase Type 0861-00, 02 Feature F0939-00
- Dual Density 1600 bpi Phase/800 bpi NRZI Type 0861-00, 02 Feature F0935-00
- W/R, R/R Simultaneity - 1600 bpi Phase; 800 bpi NRZI - Non-simultaneous Type 0861-00, 02 Feature F0934-00 and F0935-00
- W/R, R/R Simultaneity - 1600 bpi Phase; 800 bpi NRZI Type 0861-00, 02 Feature F0934-00, 01, and F0935-00
- W/R, R/R Simultaneity - 200, 556, 800 bpi NRZI Type 0861-04, 06 Feature F0934-02
- Capability for 200, 556, 800 bpi NRZI exists if UXII-C-2 Type 0861-05, 07 is within the bank.
- XVI 9-Track Type 0862-00, 01
- XVI 7-Track Type 0862-02, 03
- W/R, R/R Simultaneity Type 0862-00, 01 Feature F0936-00
- Dual density - 1600 bpi phase/800 bpi NRZI Type 0862-00, 01 Feature F0937-00
- W/R, R/R Simultaneity - 1600 bpi Phase/800 bpi NRZI Type 0862-00, 01 Feature F0936-00 and 0937-00
- W/W, W/R, R/W, R/R Simultaneity - 1600 bpi Phase/800 bpi NRZI Type 0862-00, 01 Feature F0936-00, 0936-01, 0937-00
- W/R, R/R Simultaneity - 200, 556, 800 bpi NRZI Type 0862-02, 03 Feature F0936-00
- W/W, W/R, R/W, R/R Simultaneity - 200, 556, 800 bpi NRZI Type 0862-02, 03 Feature F0936-00, 0936-01

1.4 Associated Software - This program relies on the Maintenance Control Routine (MCR) to perform program loading, parameterization, Execution, Deletion, and I/O Handling.

1.5 Reference Documents - Documents used as reference material during the development of this test are as follows:

Drawing	Rev.	Description
S-70040		9400 Processor and Console Product Description
4091622		9400 Maintenance Control Routine
	-	9400 Bootstrap Assembler on 1107/1108
4096482	C	Documentation Standard for Engineering Programming Publications
4096483		General Parameter and Message Standard for Test Programs
4091623		9400 Parameter and Message Routine
4091624		9400 Standard Subroutines
P-10052		VI-C Subsystem (9000 Series) Type 0858-XX
P-10059	A	XII/XVI Subsystem (9000 Series) Type 5017-XX, 086X-XX
T5017	3	9400 5017 XII/XVI Magnetic Tape Subsystem Test Program Description Drawing, Revision 3
Memo 12/29/67 H.B. Brown to J.P. Ashbaugh		Simulator and Monitor Mode of Operation (XII-XVI)

2. GENERAL DESCRIPTION

2.1 Program Philosophy - The test described in this document, the Uniservo XII/XVI Magnetic Tape Subsystem Control Unit test, is divided into six main sections. The first section tests the execution of basic commands and the last section tests the operation of three hardware options, Dual Access (Feature 4), Simultaneity except Write/Write (Feature 5), and Write/Write Simultaneity (Feature 6). The other four sections issue Read and Write Commands in the Simulate Mode, each section issuing commands to a different variety of (simulated) device.

Each section of the test is made up of phases. The phases are numbered consecutively throughout the test program. Each one sets up a series of expected outcomes, issues a command, and then makes a series of checks to verify that the actual outcomes match the expected outcomes. This process verifies that the command is executed correctly. (If a phase issues more than one command, all commands issued are checked.) Most of the checks are fairly standard; they are made on all or most of the commands. These checks and their expected outcomes are shown in Figure 1, Paragraph 2.3. Other checks (and their expected outcomes) are unique to a certain type of command and are listed in the phase descriptions.

If a check finds that an actual outcome does not match an expected outcome, an error condition results and an error message is displayed. Each phase has its own set of error messages. The error messages are listed in Section 3.9.3. They are numbered by phases and listed in order of occurrence of the phase which they match.

Although there may be more than one cause of error in a given phase, the phase is aborted when the first error is encountered. Therefore no more than one error message per phase is ever displayed. Some phases are dependent on preceding phases. Therefore, once an error message has been displayed, error messages from subsequent phases may not be meaningful. The error messages following the first one can be caused by the first error.

If Variable 1 (V1) is not deleted from the program, the error messages are displayed by the console. If Variable 7 (V7) is entered, the messages are displayed on the high speed printer. If Variable 4 (V4) is entered, the program stops after displaying an error message. The operator may resume the program by entering a Resume (R) parameter statement (See Paragraph 3.7.3.) or resume it by entering a Begin (B) parameter statement (See Paragraph 3.7.3.).

If Variable 14 (V14) is entered, the program cycles continuously until suspended by the entry of an End (E) parameter statement (See Paragraph 3.7.2.).

2.1.1 Basic Command Portion - Section One - The first of the six main parts of the test comprises Phases 1 through C. It executes and checks basic commands. It operates in the building-block mode; it checks the simplest commands first, and if they are executed correctly, they are then used to test other commands. Among the commands executed and checked are the Mode Set (Monitor Mode) and the Mode Set (Set Simulation Mode) Commands. These two modes remain set until Section Six of the test is executed.

2.1.2 Simulate Mode Portion - Sections Two, Three, Four, and Five - The Simulate Mode is set during the execution of Sections Two through Five. This mode setting causes each Read or Write Command issued to be sent, after decoding by the control

unit, to a portion of the control unit called the simulator. The simulator generates the responses to the commands that a tape unit would make. The type of device whose responses the simulator generates is determined by the device number which it receives. (Figure 1, Paragraph 4.3, shows the device numbers issued by this test and the simulated device which each selects.) By checking the responses of the simulator, the test program verifies that the control unit (including the simulator) is handling the commands correctly. Thus the use of the Simulate Mode allows the user to test the control unit without connecting it to a tape unit.

Most of this portion of the test executes one sequence of three commands: A Write Command, a Sense Command, and a Read Command. Each Write Command(the first command executed in each sequence) issues the same four-byte Write pattern. Upon completion of each command, data derived from the Write pattern is stored in the Cyclic Redundancy Check (CRC) Register by the control unit. (The expected data for each type of device is given in Paragraph 4.1; its derivation is given in Paragraph 4.2). The stored data provides a check on the execution of the Write Command. To obtain it, a Sense Command is issued in the Monitor Mode, causing the Monitor Sense Bytes to be sent to the Processor. Bits 6-7 of Monitor Sense Byte 3 and Bits Ø-6 of Monitor Sense Byte 4 hold the contents of the CRC Register; they are compared to the expected data pattern to verify that the two patterns are equal.

When each Read Command (the last command in each sequence) is executed, the data received is derived from the data presently in the CRC Register. If the data stored in the CRC Register as a result of the previous Write Command is incorrect, the data received as a result of the Read Command is also incorrect. (Paragraphs 4.1 and 4.2 give the expected data and its derivation.) Thus issuing a Sense Command between the Write and Read Commands checks the execution of the Write Command and also verifies that the correct data is present in the CRC Register for the execution of the Read Command.

2.1.2.1 Section Two (9-Track Phase Mode) - Section Two comprises Phases D through I. It executes two Write-Sense-Read command sequences, issuing the first sequence to Device Ø (U16 - Phase Mode) and the second to Device 1 (U12 - Phase Mode).

2.1.2.2 Section Three (9-Track NRZI) - Section Three comprises Phases J through O. It first checks the test program's parameter table for Feature 3, 9-Track NRZI. If F3 is not entered, the test skips two sections, jumping to Phase 1F (Section Five). If Feature 3 is present, the test checks the two 9-Track NRZI devices (simulated) by issuing two Write-Sense-Read command sequences, first to Device 2 (U16 - NRZI Mode) and then to Device 3 (U12 - NRZI Mode).

2.1.2.3 Section Four (7-Track with 9-Track NRZI) - Section Four and Section Five are mutually exclusive. They both test 7-Track devices, Section Four if the subsystem also includes Feature 3 (9-Track NRZI) and Section Five if the subsystem does not include Feature 3.

Section Four, when executed, follows Section Three. It comprises Phases P through 1E. Phase P checks the test program's parameter table for Feature 1 (7-Track). If F1 is not entered, the test jumps to Phase 26 (Section Six). If F1 is present, the test issues commands to two 7-Track devices, Device 4 and Device 5.

Phases P through 11 issue three Write-Sense-Read command sequences to Device 4 (U16 - 7-Track). However, in order to test the Data Translator and the Data

Converter, four Mode Set Commands are issued. The first one, issued before the second Read Command (the Read Command in the second command sequence), sets the Data Translator. The second Mode Set Command is issued after the second Read Command and resets (turns off) the Data Translator. The third and fourth Mode Set Commands are issued before and after the Read Command in the third command sequence; they set and reset the Data Converter.

Phases 12 through 1E issue commands to Device 5 (U12 - 7-Track). Otherwise they are identical to Phases P through 11.

2.1.2.4 Section Five (7-Track without 9-Track NRZI) - When executed, Section Five follows Section Two. It is begun when Section Three finds that Feature 3 (9-Track NRZI) is not present but is otherwise identical to Section Four. The first phase, Phase 1F, checks the test program's parameter table for Feature 1 (7-Track). If it is not present, the test program jumps to Phase 26 (Section 6). Otherwise, Phases 1F through 25 are executed.

2.1.3 Dual Access and Simultaneity Portion - Section Six - Section Six tests Feature 4 (Dual Access), Feature 5 (Simultaneity except Write/Write) and Feature 6 (Write/Write Simultaneity). It comprises Phases 26 through 2F, 1I through 2M, and 2G (out of order). (Phase 2H is nonexistent.)

Most of this portion of the test does not operate in the Simulate Mode. It issues commands to actual devices, the Dual Access Test to one and the Simultaneity Test to two. Because of restrictions imposed by the Parameter and Message Routine (PMR) and by the test program, each parameter entry may specify only one channel, one subchannel, and two devices. The program assumes that the tape unit with the lower device number (the third digit in the device address) is on the specified channel and that the higher numbered device is on the opposite (not entered) channel.

Therefore, to specify by parameter entry the two tape units to be used for the Simultaneity Test, the operator enters the two device addresses of the tape units (which contain the two subchannel designators) and the channel number of the lower numbered device. If the operator enters two device addresses with different subchannel designators (two different subchannel numbers) the PMR overwrites the first one entered with the second. Entry of two different channel numbers has the same result. If the operator specifies more than two devices, all but the two with the lowest numbers are ignored by the test program.

Phases 26 through 29 are preparatory. They reset the Simulate Mode; the remainder of the test operates in the Monitor Mode only. Phase 26 issues a Mode Set (Reset Simulate Mode) Command which resets both the Simulate Mode and the Monitor Mode, and Phase 28 issues a Mode Set (Set Monitor Mode) Command which sets the Monitor Mode again.

2.1.3.1 Dual Access Test - Installation of the Dual Access Feature provides the control unit with a second channel interface, thus allowing it to be addressed by either of the selector channels. This feature is tested by Phases 2A through 2F. The test verifies that the channel interfaces reserve the control unit in response to a Sense/Reserve Command (the channel interface which issues the Sense/Reserve Command is locked on to the control unit, thus preventing operations issued on the other channel from being initiated) and release the control unit in response to a Sense/Release Command.

All commands are issued to the lower numbered of the devices specified by parameter entry. Phase 2A first verifies that F4 (Dual Access) is entered in the test program's parameter table (if it is not, the test program jumps to Phase 2I) and then issues a Sense/Reserve Command on the primary channel. Phase 2B issues a Sense Command on the opposite (secondary) channel and expects a response indicating that the control unit is busy (a status code equal to 5Ø received from the control unit). This response verifies that the control unit has been reserved for the primary channel interface as a result of the Sense/Reserve Command. Phase 2C then issues a Sense/Release command, causing release of the control unit from the primary channel interface. The test then waits for a Control Unit End Interrupt from the secondary channel indicating that the control unit has been released.

Phases 2D through 2F issue the same sequence of commands on the opposite channels. Phase 2D issues a Sense/Reserve Command on the secondary channel, Phase 2E issues a Sense Command on the primary channel, and Phase 2F issues a Sense/Release Command on the secondary channel.

2.1.3.2 Simultaneity Test - Phases 2I through 2M and Phase 2G comprise the Simultaneity Test. They are the last five phases in the test program. Phase 2I checks the test program's parameter table for Feature 5. If it is entered, Phases 2I through 2L and Phase 2G are executed. Phase 2M checks for Feature 6 and is executed if F6 also is entered.

Phase 2I issues a Write Command to the lower numbered of the two devices specified by parameter entry. The execution of this command positions the tape so that the tape unit can execute the Read Backward Command issued to it by Phase 2J. Phase 2G issues an Erase Command to each of the specified devices. It is not part of the test but is made necessary by a peculiarity of the control unit.

The remaining phases issue Read and Write Commands to the two specified devices. Although the data read or written is not checked, the phases make the standard checks on the execution of the commands. These checks verify that the two control units handled the commands correctly. Phase 2J checks Write/Read Simultaneity, Phase 2K tests Write/Read Simultaneity (devices reversed) and Phase 2L tests Read/Read Simultaneity. If Feature 6 is present, Phase 2M then tests Write/Write Simultaneity.

2.2 Test Description - This test is divided into 96 phases. Each phase issues one or more commands and then checks for certain expected results.

The following paragraphs describe each phase separately, listing each command a phase issues and all the unique checks it makes. The standard checks a phase makes are given in Table 1.

2.2.1 Section One - (Basic Commands) -

Phase 1 issues eight Test I/O Commands. Each command uses a different one of the eight possible codes for the Test I/O Command. A check verifies that no change occurred in the Byte Count in the CSW.

Phase 2 issues a Mode Set (No-Op) Command. This phase verifies that a Mode Set Command can be executed correctly.

Phase 3 issues a Sense Command (Byte Count = 5), thus verifying that a Sense Command can be executed correctly. It saves the Sense data received for a check in Phase 4. Phase 2 is repeated.

Phase 4 issues a Sense Command (Byte Count = 5). A check compares the Sense data received in Phase 4 to the Sense data received in Phase 3. A match verifies that the second Phase 2 Mode Set (No-Op) Command did not alter the Sense data.

Phase 5 issues a Sense Command with the Byte Count equal to seven. A check verifies that the final Byte Count in the proper CSW equals two and thus that no more than five sense bytes were transferred.

Phase 6 issues a Mode Set (Set Monitor Mode) Command.

Phase 7 verifies that as a result of setting the Monitor Mode in Phase 6 the control unit will send out Monitor Sense data in response to a Sense Command. The phase executes a Sense Command and then verifies that Bit 1 of Byte 1 equals 1. (If this bit equals Ø, Sense data, not Monitor Sense data, was sent out by the 5Ø17 Control Unit.)

Phase 8 issues an Inhibit Status Command. This phase verifies that an Inhibit Status Command can be executed correctly.

Phase 9 issues a Re-Set Inhibit Status Command.

Phase A checks the execution of the Re-Set Inhibit Status Command executed in Phase 9. It executes a Sense Command and then verifies that the Inhibit Status In bit has been reset (Bit 5, Monitor Sense Byte 3, equals Ø).

Phase B issues a Mode Set (Set Device Simulation Mode) Command. The Device Simulation Mode remains set for most of the test.

Phase C verifies that the Device Simulation Mode is set. It issues a Sense Command and then verifies that Bit 7 of Monitor Sense Byte 1 (Device Simulation Mode) is set.

2.2.2 Section Two (9-Track Phase Mode) - All Simulated Write and Simulated Read operations use a Byte Count of 4.

Phase D issues a Write Command to Device Ø.

Phase E issues a Sense Command (Byte Count = 5). A check verifies that Bits 6 and 7 of Monitor Sense Byte 3 and Bits Ø through 6 of Monitor Sense Byte 4 equal $ØØ_{16}$.

Phase F issues a Read Command to Device Ø. A check verifies that the data bytes received equal $ØØFFØØFF_{16}$.

Phase G issues a Write Command to Device 1.

Phase H issues a Sense Command (Byte Count = 5). A check verifies that Bits 6 and 7, Monitor Sense Byte 3, and Bits Ø through 6, Monitor Sense Byte 4, equal $ØØ_{16}$.

Phase I issues a Read Command to Device 1. A check verifies that the data received equals $ØØFFØØFF_{16}$.

2.2.3 Section Three (9-Track NRZI) -

Phase J checks the test program's parameter table for Feature 3 (9-Track NRZI). If F3 is not entered, the test program jumps to Phase 1F. Otherwise, Phase J issues a Write Command to Device 2.

Phase K issues a Sense Command (Byte Count = 5). A check verifies that Bits 6 and 7, Monitor Sense Byte 3, and Bits Ø through 6, Monitor Sense Byte 4, equal $B4_{16}$.

Phase L issues a Read Command to Device 2. A check verifies that the data received equals $638DFAC1_{16}$.

Phase M issues a Write Command to Device 3.

Phase N issues a Sense Command (Byte Count = 5). A check verifies that Bits 6 and 7, Monitor Sense Byte 3, and Bits Ø through 6, Monitor Sense Byte 4, equal $B4_{16}$.

Phase O issues a Read Command to Device 3. A check verifies that the data received equals $638DFAC1_{16}$.

2.2.4 Section Four (7-Track if 9-Track NRZI Present) -

Phase P checks the test program's parameter table for Feature 1 (7-Track). If it is not entered, the test jumps to Phase 26 (Section 6). Otherwise, Phase P issues a Write Command to Device 4.

Phase Q issues a Sense Command (Byte Count = 5). A check verifies that Bits 6 and 7, Monitor Sense Byte 3, and Bits Ø through 6, Monitor Sense Byte 4, equal 39_{16}.

Phase R issues a Read Command to Device 4. A check verifies that the data received equals $3B321624_{16}$.

Phase S issues a Write Command to Device 4.

Phase T issues a Sense Command (Byte Count = 5). A check verifies that Bits 6 and 7, Monitor Sense Byte 3, and Bits Ø through 6, Monitor Sense Byte 4, equal 39_{16}.

Phase U issues a Mode Set Command (800 bpi, odd parity, data converter off, data translator on), setting the data translation mode.

Phase V issues a Read Command to Device 4. A check verifies that the data received equals $4BC2E6D4_{16}$.

Phase W issues a Mode Set Command (800 bpi, odd parity, data converter off, data translator off), resetting the data translation mode (turning off the data translator).

Phase X issues a Write Command to Device 4.

Phase Y issues a Sense Command (Byte Count = 5). A check verifies that Bits 6 and 7, Monitor Sense Byte 3, and Bits Ø through 6, Monitor Sense Byte 4, equal 39_{16}.

Phase Z issues a Mode Set Command (800 bpi, odd parity, data converter on, data translator off), setting the data conversion mode.

Phase 1Ø issues a Read Command to Device 4. A check verifies that the data received equals $EF25A4F5_{16}$.

Phase 11 issues a Mode Set Command (800 bpi, odd parity, data converter off, data translator off) resetting the data conversion mode (turning off the data converter).

Phase 12 issues a Write Command to Device 5.

Phase 13 issues a Sense Command (Byte Count = 5). A check verifies that Bits 6 and 7, Monitor Sense Byte 3, and Bits Ø through 6, Monitor Sense Byte 4, equal 39_{16}.

Phase 14 issues a Read Command to Device 5. A check verifies that the data received equals $3B321624_{16}$.

Phase 15 issues a Write Command to Device 5.

Phase 16 issues a Sense Command (Byte Count = 5). A check verifies that Bits 6 and 7, Monitor Sense Byte 3, and Bits Ø through 6, Monitor Sense Byte 4, equal 39_{16}.

Phase 17 issues a Mode Set Command (800 bpi, odd parity, data converter off, data translator on) to turn on the data translator.

Phase 18 issues a Read Command to Device 5. A check verifies that the data received equals $4BC2E6D4_{16}$.

Phase 19 issues a Mode Set Command (800 bpi, odd parity, data converter off, data translator off) to turn off the data translator.

Phase 1A issues a Write Command to Device 5.

Phase 1B issues a Sense Command (Byte Count = 5). A check verifies that Bits 6 and 7, Monitor Sense Byte 3, and Bits Ø through 6, Monitor Sense Byte 4, equal 39_{16}.

Phase 1C issues a Mode Set Command (800 bpi, odd parity, data converter on, data translator off), setting the data conversion mode (turning on the data converter).

Phase 1D issues a Read Command to Device 5. A check verifies that the data received equals $EF25A4F5_{16}$.

Phase 1E issues a Mode Set Command (800 bpi, odd parity, data converter off, data translator off), resetting the data conversion mode (turning off the data converter).

2.2.5 Section Five (7-Track if 9-Track NRZI Not Present) -

Phase 1F checks the test program's parameter table for Feature 1 (7-Track). If it is not entered, the test jumps to Phase 26 (Section 6). Otherwise Phase 1F issues a Write Command to Device 4.

Phase 1G issues a Sense Command (Byte Count = 5). A check verifies that Bits 6 and 7, Monitor Sense Byte 3, and Bits Ø through 6, Monitor Sense Byte 4, equal $3F_{16}$.

Phase 1H issues a Read Command to Device 4. A check verifies that the data received equals $3F3F3F3F_{16}$.

Phase 1I issues a Write Command to Device 4.

Phase 1J issues a Sense Command (Byte Count = 5). A check verifies that Bits 6 and 7, Monitor Sense Byte 3, and Bits Ø through 6, Monitor Sense Byte 4, equal $3F_{16}$.

Phase 1K issues a Mode Set Command (800 bpi, odd parity, data converter off, data translator on) to set the data translation mode (turn on the data translator).

Phase 1L issues a Read Command to Device 4. A check verifies that the data received equals $4F4F4F4F_{16}$.

Phase 1M issues a Mode Set Command (800 bpi, odd parity, data converter off, data translator off) to reset the data translation mode (turn off the data translator).

Phase 1N issues a Write Command to Device 4.

Phase 1O issues a Sense Command (Byte Count = 5). A check verifies that Bits 6 and 7, Monitor Sense Byte 3, and Bits Ø through 6, Monitor Sense Byte 4, equal $3F_{16}$.

Phase 1P issues a Mode Set Command (800 bpi, odd parity, data converter on, data translator off) to set the data conversion mode (turn on the data converter).

Phase 1Q issues a Read Command to Device 4. A check verifies that the data received equals $FFFFFFFF_{16}$.

Phase 1R issues a Mode Set Command (800 bpi, odd parity, data converter off, data translator off) to reset the data conversion mode (turn off the data converter).

Phase 1S issues a Write Command to Device 5.

Phase 1T issues a Sense Command (Byte Count = 5). A check verifies that Bits 6 and 7, Monitor Sense Byte 3, and Bits Ø through 6, Monitor Sense Byte 4, equal $3F_{16}$.

Phase 1U issues a Read Command to Device 5. A check verifies that the data received equals $3F3F3F3F_{16}$.

Phase 1V issues a Write Command to Device 5.

Phase 1W issues a Sense Command (Byte Count = 5). A check verifies that Bits 6 and 7, Monitor Sense Byte 3, and Bits Ø through 6, Monitor Sense Byte 4, equal $3F_{16}$.

Phase 1X issues a Mode Set Command (800 bpi, odd parity, data converter off, data translator on) to set the data translation mode (turn on the data translator).

Phase 1Y issues a Read Command to Device 5. A check verifies that the data received equals $4F4F4F4F_{16}$.

Phase 1Z issues a Mode Set Command (800 bpi, odd parity, data converter off, data translator off) to reset the data translation mode (turn off the data translator).

Phase 21 issues a Write Command to Device 5.

Phase 22 issues a Sense Command (Byte Count = 5). A check verifies that Bits 6 and 7, Monitor Sense Byte 3, and Bits Ø through 6, Monitor Sense Byte 4, equal $3F_{16}$.

Phase 23 issues a Mode Set Command (800 bpi, odd parity, data converter on, data translator off), to set the data conversion mode (turn on the data converter).

Phase 24 issues a Read Command to Device 5. A check verifies that the data received equals $FFFFFFFF_{16}$.

Phase 25 issues a Mode Set Command (800 bpi, odd parity, data converter off, data translator off), to reset the data conversion mode (turn off the data converter).

2.2.6 Section Six (Dual Access Test and Simultaneity Test) -

Phase 26 issues a Mode Set Command (Reset Simulate Mode). This command resets both the Simulate Mode and the Monitor Mode; the test is no longer operating in either mode.

Phase 27 verifies that the Monitor Mode has been reset. It issues a Sense Command and then checks Sense Byte 1. If Bit 1 equals Ø, Sense data, not Monitor Sense data was received. If Bit 1 of Sense Byte 1 equals 1, Monitor Sense data was received and the Monitor Mode is not reset.

Phase 28 issues a Mode Set Command (Set Monitor Mode) to set the Monitor Mode.

Phase 29 verifies that the Monitor Mode was set in Phase 28. It executes a Sense Command and then verifies that Bit 1 of Byte 1 of the data received equals 1. (If Bit 1 of Byte 1 equals Ø, Sense data, not Monitor Sense data, was received and the Monitor Mode is not set.)

2.2.6.1 Dual Access - Phases 2A through 2F issue commands to the lower numbered of the devices selected by parameter entry.

Phase 2A checks the test program's parameter table for Feature 4 (Dual Access). If it is not present, the test jumps to Phase 2I. Otherwise, Phase 2A issues a Sense/Reserve Command on the primary channel. A check verifies that Bit 6 of Monitor Sense Byte 1 equals 1 (Channel Interface Reserved).

Phase 2B issues a Sense Command on the secondary channel. A check verifies that a status code equal to 5Ø (Busy and Status Modifier Bits set) is stored in the CAW. Reception of this status code verifies that the control unit has been reserved by the primary channel as a result of the Sense/Reserve Command executed in Phase 2A.

Phase 2C issues a Sense/Release Command on the primary channel. A check verifies that Bit 6 of Monitor Sense Byte 1 is reset to Ø, thus indicating that the channel has released the control unit.

The test program waits for a Control Unit End Interrupt from the secondary channel before proceeding.

Phase 2D issues a Sense/Reserve Command on the secondary channel. A check verifies that Bit 6 of Monitor Sense Byte 1 equals 1 (Channel Interface Reserved).

Phase 2E issues a Sense Command on the primary channel. A check verifies that a status code of 5Ø (Busy and Status Modifier Bits set) is stored in the CAW. Reception of this status code verifies that the control unit has been reserved by the secondary channel as a result of the Sense/Reserve Command executed in Phase 2D.

Phase 2F issues a Sense/Release Command on the secondary channel. A check verifies that Bit 6 of Monitor Sense Byte 1 is reset to Ø, thus indicating that the secondary channel has released the control unit.

The test program waits for a Control Unit End Interrupt from the primary channel before proceeding.

2.2.6.2 Simultaneity Test -

Phase 2I checks the test program's parameter table for Feature 5 (Simultaneity except Write/Write). If it is not present, the test terminates. Otherwise, Phase 2I issues a Write Command (Byte Count = 256) to the lower numbered device (of the two specified by parameter entry).

Phase 2J issues a Write Command (Byte Count = 256) to the higher numbered device on the unspecified (by parameter entry) channel. Upon completion of the SIO instruction (CC = Ø), the program switches to the specified channel and the lower numbered device and issues a Read Backward Command (Byte Count = 256). When the second SIO instruction is completed (CC = Ø), the program waits for two interrupts before checking for the following conditions.

1) Two interrupts generated
2) A Status Code of $ØC_{16}$ stored in both CSW's.
3) A residual Byte Count of Ø in both CSW's.

Phase 2G has no testing function; its presence is necessitated by a peculiarity of the control unit. It issues an Erase Command to one device. When the SIO instruction is completed (a check verifies that the Condition Code equals Ø), the program switches to the opposite channel and issues an Erase Command to the other device. When the second SIO instruction is completed (CC = Ø), the test waits for two interrupts and then checks for the following conditions.

1) A Status Code of $8Ø_{16}$ (Channel End) stored in both CSW's
2) A residual Byte Count of Ø in both CSW's

Following these checks, the test waits for two more interrupts and then checks for the following conditions.

1) A Status Code of $Ø4_{16}$ (Device End) stored in both CSW's
2) A residual Byte Count of Ø in both CSW's

Phase 2K issues a Write Command (Byte Count = 256) to the lower numbered device. Upon completion of the SIO instruction (a check verifies that the Condition Code equals Ø), the program switches to the opposite channel and the higher numbered device and issues a Read Backward Command (Byte Count = 256). When the second SIO instruction is completed (CC = Ø), the program waits for two interrupts and then checks for the following conditions.

1) Two interrupts generated
2) A Status Code of $\emptyset C_{16}$ stored in both CSW's
3) A residual Byte Count of $\emptyset$ in both CSW's

Phase 2L issues a Read Backward Command (Byte Count = 256) to the lower numbered device. Upon completion of the SIO instruction (CC = $\emptyset$), the program switches to the opposite channel and the higher numbered device and issues a Read Forward Command (Byte Count = 256). When the second SIO instruction is completed (CC = $\emptyset$), the program waits for two interrupts and then checks for the following conditions.

1) Two interrupts generated
2) A Status Code of $\emptyset C_{16}$ stored in both CSW's
3) A residual Byte Count of $\emptyset$ in both CSW's

Phase 2M checks the test program's parameter table for Feature 6 (Write/Write Simultaneity). If it is not present, the test terminates. Otherwise Phase 2M tests the ability of the control unit to execute Write Commands simultaneously. It issues a Write Command (Byte Count = 256) to the lower numbered device. Upon completion of the SIO instruction (CC = $\emptyset$), the program switches to the opposite channel and higher numbered device and issues another Write Command (Byte Count = 256). When the second SIO instruction is completed (CC = $\emptyset$), the program waits for two interrupts and then checks for the following conditions.

1) Two interrupts generated
2) A Status Code of $\emptyset C_{16}$ stored in both CSW's
3) A residual Byte Count of $\emptyset$ in both CSW's

When the checks are completed, the test terminates unless V14 (Cycle Test) is entered.

2.3 Figure 1 - This table lists the standard checks that each phase makes. Unique checks, those made only after one type of command, are given in the phase description. The last five phases (Phases 2J through 2M) are not included in the table.

The left column in the table contains the phase numbers; each of the other column headings lists an outcome for which many phases check. When a specific phase checks for one of these outcomes, the square in the table corresponding to the phase and the outcome contains either an X or a character which further defines the outcome for which the check is made. The characters in the column headed "INTERRUPT GENERATED?" denote whether a check is made for an interrupt (Y) or whether a check is made to verify that an interrupt is not generated (No). The character in the column headed "SIO CONDITION CODE" is the Condition Code checked for, $\emptyset$ or 1. The column headed "STORAGE LOCATION OF A STATUS CODE OF $\emptyset C_{16}$" tells whether a phase checks for a status code of $\emptyset C_{16}$ stored in the Channel Address Word (CAW) or whether a phase checks for a status code of $\emptyset C_{16}$ stored in the Channel Status Word (CSW).

PHASE NUMBER	INTERRUPT GENERATED?	SIO CONDITION CODE	A PSW INTERRUPT CODE EQUAL TO THE ADDRESS IN THE SIO INSTRUCTION	STORAGE LOCATION OF A STATUS CODE OF $\emptyset C_{16}$	A FINAL BYTE COUNT OF Ø IN THE PROPER CSW	SENSE DATA NOT EQUAL TO Ø RECEIVED
1	No	Ø				
2	No	1		CAW		
3	Y	Ø	X	CSW	X	X
2	No	1		CAW		
4	Y	Ø	X	CSW	X	X
5	Y	Ø	X	CSW		X
6	No	1		CAW		
7	Y	Ø	X	CSW	X	X
8	No	Ø				
9	No	Ø				
A	Y	Ø	X	CSW	X	X
B	No	1		CAW		
C	Y	Ø	X	CSW	X	X
D	Y	Ø	X	CSW	X	
E	Y	Ø	X	CSW	X	X
F	Y	Ø	X	CSW	X	
G	Y	Ø	X	CSW	X	
H	Y	Ø	X	CSW	X	X
I	Y	Ø	X	CSW	X	
J	Y	Ø	X	CSW	X	
K	Y	Ø	X	CSW	X	X
L	Y	Ø	X	CSW	X	
M	Y	Ø	X	CSW	X	
N	Y	Ø	X	CSW	X	X
O	Y	Ø	X	CSW	X	
P	Y	Ø	X	CSW	X	
Q	Y	Ø	X	CSW	X	X
R	Y	Ø	X	CSW	X	
S	Y	Ø	X	CSW	X	
T	Y	Ø	X	CSW	X	X

PHASE NUMBER	INTERRUPT GENERATED?	SIO CONDITION CODE	A PSW INTERRUPT CODE EQUAL TO THE ADDRESS IN THE SIO INSTRUCTION	STORAGE LOCATION OF A STATUS CODE OF $\emptyset C_{16}$	A FINAL BYTE COUNT OF Ø IN THE PROPER CSW	SENSE DATA NOT EQUAL TO Ø RECEIVED
U	No	1		CAW		
V	Y	Ø	X	CSW	X	
W	No	1		CAW		
X	Y	Ø	X	CSW	X	
Y	Y	Ø	X	CSW	X	X
Z	No	1		CAW		
1Ø	Y	Ø	X	CSW	X	
11	No	1		CAW		
12	Y	Ø	X	CSW	X	
13	Y	Ø	X	CSW	X	X
14	Y	Ø	X	CSW	X	
15	Y	Ø	X	CSW	X	
16	Y	Ø	X	CSW	X	X
17	No	1		CAW		
18	Y	Ø	X	CSW	X	
19	No	1		CAW		
1A	Y	Ø	X	CSW	X	
1B	Y	Ø	X	CSW	X	X
1C	No	1		CAW		
1D	Y	Ø	X	CSW	X	
1E	No	1		CAW		
1F	Y	Ø	X	CSW	X	
1G	Y	Ø	X	CSW	X	X
1H	Y	Ø	X	CSW	X	
1I	Y	Ø	X	CSW	X	
1J	Y	Ø	X	CSW	X	X
1K	No	1		CAW		
1L	Y	Ø	X	CSW	X	
1M	No	1		CAW		

PHASE NUMBER	INTERRUPT GENERATED?	SIO CONDITION CODE	A PSW INTERRUPT CODE EQUAL TO THE ADDRESS IN THE SIO INSTRUCTION	STORAGE LOCATION OF A STATUS CODE OF $\emptyset C_{16}$	A FINAL BYTE COUNT OF $\emptyset$ IN THE PROPER CSW	SENSE DATA NOT EQUAL TO $\emptyset$ RECEIVED
1N	Y	$\emptyset$	X	CSW	X	
1O	Y	$\emptyset$	X	CSW	X	X
1P	No	1		CAW		
1Q	Y	$\emptyset$	X	CSW	X	
1R	No	1		CAW		
1S	Y	$\emptyset$	X	CSW	X	
1T	Y	$\emptyset$	X	CSW	X	X
1U	Y	$\emptyset$	X	CSW	X	
1V	Y	$\emptyset$	X	CSW	X	
1W	Y	$\emptyset$	X	CSW	X	X
1X	No	1		CAW		
1Y	Y	$\emptyset$	X	CSW	X	
1Z	No	1		CAW		
21	Y	$\emptyset$	X	CSW	X	
22	Y	$\emptyset$	X	CSW	X	X
23	No	1		CAW		
24	Y	$\emptyset$	X	CSW	X	
25	No	1		CAW		
26	No	1		CAW		
27	Y	$\emptyset$	X	CSW	X	X
28	No	1		CAW		
29	Y	$\emptyset$	X	CSW	X	X
2A	Y	$\emptyset$	X	CSW	X	X
2B		1				
2C	Y	$\emptyset$	X	CSW	X	X
2D	Y	$\emptyset$	X	CSW	X	X
2E		1				
2F	Y	$\emptyset$	X	CSW	X	X
2I	Y	$\emptyset$	X	CSW	X	

3. OPERATING PROCEDURES

3.1 Initialization - Mount scratch tapes on the two devices to be used for the Simultaneity Test.

3.2 Program Loading -

- Press the ATTENTION key - the console responds with the @ sign, a time stamp, and a space.
- Type in RU - the console responds with N and a space.
- Type in the program name - T5Ø17C - and press the EOM key. The following statement now appears on the console.

  @hh:mm RUN T5Ø17C©

- When the job is loaded, the following message appears on the console. It gives the test program's job number and starting address.

  JOB j, T5Ø17C LOADED AT (address)

3.3 Program Starting - The program is started as soon as it is loaded. The following message appears on the console.

@hh:mm A j T5Ø17C ENTER PARAMETERS

This is a good time (after the program is started and before it is begun) to disable the timer. It is preferable that the program be run without it.

3.4 Program Modifying - The program is modified by entry of parameter statements. The parametersmay be entered at any time during the operation of the test; however, the test program processes parameters only when recycling.

Parameters entered while the program is testing are not processed until the program completes the last phase. Therefore, the program cannot be stopped (suspended) by parameter entry during the execution of the test; the program stops testing only if an error occurs with V7 (Stop on Error) entered. Parameters entered while the program is suspended (for any reason) are processed immediately.

3.5 Parameters - The standard parameters or program designators are divided into three categories, Action Designators, Equipment Designators, and Test Designators.

3.5.1 Action Designators - The Action Designators (listed below) tell the test program what action to perform.

A = Add
B = Begin
D = Delete
E = Suspend
R = Resume
V = View

3.5.2 Equipment Designators - The Equipment Designators (listed below) describe the equipment to be tested.

Cn = Channel Number
Ann,n = A three-character device address consisting of, in order, the alpha character (arbitrarily assigned) which designates the subsystem's control unit, a hexadecimal number which is the subchannel address of the control unit, and a hexadecimal number which specifies a selected device (unit) in the subsystem.

Fn = Feature number, where

F1 = 7-Track
F2 = Data Conversion
F3 = 9-Track NRZI
F4 = Dual Access
F5 = Simultaneity except Write/Write
F6 = Write/Write Simultaneity

3.5.3 Test Designators - The Test Designators (listed below) modify the MAR's testing procedure.

Vn = Variable (Program Option), where

V1 = Display Error Messages (Available on load)
V4 = Stop on Error
V7 = Route Error Messages to the High Speed Printer
V14 = Cycle the Test

3.6 Parameter Notes and Restrictions -

1) Entry of the Delete (D) Action Designator deletes all parameters previously entered, enabling V1.

2) A number sign (#) precedes all device addresses; it indicates to the PMR that a device address follows.

3) A period (.) separates parameter sentences.

4) Before entering a Begin (B) Action Designator, the operator must always clear the control unit.

3.7 Parameter Entries - Equipment and Test Designators are added to the test program's parameter table by entry of a parameter statement with the following format.

A Cn Fn,n Vn,n:Ann,n⊛

Each parameter statement may contain as many of the available features (Fn) or program options (Vn) as desired by the operator. However, execution of the test program requires entry of only one channel number (Cn), one subchannel designator (the second digit in the device address, Ann), and two device numbers (the third digit in the device address), and due to restrictions imposed by the Parameter and

Message Routine (PMR) and by the test program, no more of these parameters should ever be entered unless the operator is correcting an error (See Paragraph 3.7.1). Otherwise, if more of these parameters are entered (without deletion of those previously entered), the operator's intentions are misinterpreted by the PMR and by the test program.

Execution of any portion of Sections One through Five of the test program requires entry of a channel number and one device address. Execution of the Simultaneity Test requires entry of a channel number and two device addresses. No other channel, subchannel or device parameters are ever needed.

Two channel numbers or two differing subchannel designators should never be entered in the same parameter sentence. If the format given above is followed, two channel or subchannel numbers cannot be entered. If, however, the format is not followed, and two differing channel or subchannel numbers are entered, the PMR overwrites the first parameter entered with the second. For instance, the following parameter statement contains two differing subchannel numbers.

A C1 F4,5:#A6Ø,B34⊛

If it is entered, it is interpreted as follows:

A C1 F4,5:#B3Ø,B34⊛ (or as A C1 F4,5:#B3Ø,4⊛

If more than two device designators are entered, all but the two lowest (numerically) are ignored by the test program. For instance, the following parameter statement contains three device designators.

A C1, F4,5:#A6Ø,C,4⊛

If it is entered, it is interpreted as follows:

A C1, F4,5:#A6Ø,4⊛

3.7.1 Recovery Procedures - If incorrect Equipment or Test Designators are entered, one of the following recovery procedures is used.

If an incorrect channel number is entered, the operator enters another channel number, overwriting the incorrect channel number.

If an incorrect subchannel designator is entered, but the device designators are correct, the operator simply enters another device address using the correct subchannel designator and the previously entered device designators. The correct subchannel designator will overwrite the incorrect one.

Any parameter entry error is corrected by entry of the Delete (D) Designator and a period (signifying the end of a parameter sentence) or a stop code (D. or D⊛), followed by entry of the correct parameters (in the format shown in Paragraph 3.7).

3.7.2 Program Stopping - The following two entries stop the test program. Because parameter entries are not processed until the test program recycles, these entries will not stop the program until the last phase of the test has been executed. Therefore, they are not needed unless V14 (Cycle the Test) is entered.

E⊕ Entry of this statement stops the program without a console indication.

D⊕ Entry of this statement deletes all parameters from the test program's parameter table. The program is stopped and the following message is displayed on the console.

Dhh:mm j T5Ø17C LACKS CHANNEL

3.7.3 Program Starting and Restarting - The Begin (B) and Resume (R) Action Designators are used to start and restart the test program. Before the Begin Action Designator can be entered, the operator must clear the control unit.

The following parameter entry initially starts the test program.

B⊕

The following two parameter entries restart the test program.

B⊕ Entry of this statement restarts the program from the initial starting point.

R⊕ Entry of this statement restarts the program from the point at which it stopped. (The effect of this entry does not differ from that of B⊕ unless the program stopped because of encountering an error with V4 entered.)

3.8 Program Termination - To remove the program from storage, submit a Cancel directive to MCR as follows:

CANCEL j (j = job number)

3.9 Message Descriptions - The messages supplied by the test program are divided into three groups: Parameter Error Messages, Information Messages, and Subsystem Error Messages. They are displayed either on the console or, if V7 is entered, by the printer.

3.9.1 Parameter Error Messages -

1. Lacks Channel -

Cause:	The program does not have a valid channel assignment.
Program Action:	The program displays the error message and waits for more parameters.
Example:	Dhh:mmj T5Ø17C LACKS CHANNEL.
Operator Action:	Entry of a parameter statement which contains a channel number.

2. Lacks Subchannel -

Cause:	The program does not have a valid subchannel assignment.
Program Action:	The program displays the error message and waits for more parameters.
Example:	Dhh:mmj T5Ø17C LACKS SUBCHANNEL

Operator Action: Entry of a parameter statement which includes a sub-channel assignment.

3.9.2 Information Message -

Error Stop -

Cause: The program encountered an error with V4 (Stop on Error) entered.

Program Action: The program displays the message and stops.

Message: Dhh:mmj T5Ø17C STOPPED ON ERROR

3.9.3 Subsystem Error Messages - All Subsystem Error Messages except those generated by the Simultaneity Test possess the following format.

Dhh:mmj T5Ø17C ERR XXX STATUS=AXBX

AX is the Status Code received from channel 1 and BX is the Status Code received from channel 2.

When an error is encountered during the Simultaneity Test, the test program attempts to obtain the Sense Data and the Monitor Sense Data for each channel. If the attempt is unsuccessful, the error message possesses the same format as those generated by the rest of the test program. If the Sense and Monitor Sense Data is obtained, it is incorporated in the error message, which then possesses the following format.

Dhh:mmj T5Ø17C ERR XXX STATUS=AXBX

CH1 SB CH1 MB

CH2 SB CH2 MB

In either type of Subsystem Error Message, XXX is one of the messages in the following list. The messages contain a number and a phrase. The first digit of two or the first two digits of three of the number correspond to a phase number. The phrase denotes the error causing the message.

The messages are listed in groups; each group contains the messages for one particular phase. The groups are listed in the same order as the matching phases.

```
*****************************************************************************
*
*  CONTROL UNIT TEST ERROR MESSAGES
*****************************************************************************
* 10 - UNEXPECTED STATUS ON TIO
* 11 - UNEXPECTED INTERRUPT ON TIO
* 12 - CC OF 3 ON TIO
* 13 - BYTE COUNT CHANGED ON TIO
*
* 20 - CC OF 8 ON NO-OP
* 21 - UNEXPECTED INTERRUPT ON NO-OP
* 22 - CC OF 3 ON NO-OP
* 23 - STATUS NOT OC ON NO-OP
*
* 30 - CC OF 1 ON SENSE
* 31 - STATUS NOT OC ON SENSE
* 32 - CC OF 3 ON SENSE
* 33 - INTERRUPT ADDRESS ERROR ON SENSE
* 34 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* 35 - INPUT SENSE BYTES ALL ZEROES
*
* 40 - CC OF 1 ON SENSE
* 41 - STATUS NOT OC ON SENSE
* 42 - CC OF 3 ON SENSE
* 43 - INTERRUPT ADDRESS ERROR ON SENSE
* 44 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* 45 - INPUT SENSE BYTES ALL ZEROES
* 46 - SENSE BYTES CHANGED AS RESULT OF NO-OP
*
* 50 - CC OF 1 ON SENSE
* 51 - STATUS NOT OC ON SENSE
* 52 - CC OF 3 ON SENSE
* 53 - INTERRUPT ADDRESS ERROR ON SENSE
* 54 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 7)
* 55 - INPUT SENSE BYTES ALL ZEROES
*
* 60 - CC OF 0 ON SET MONITOR MODE
* 61 - UNEXPECTED INTERRUPT ON SET MONITOR MODE
* 62 - CC OF 3 ON SET MONITOR MODE
* 63 - STATUS NOT OC ON SET MONITOR MODE
*
* 70 - CC OF 1 ON SENSE
* 71 - STATUS NOT OC ON SENSE
* 72 - CC OF 3 ON SENSE
* 73 - INTERRUPT ADDRESS ERROR ON SENSE
* 74 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* 75 - INPUT SENSE BYTES ALL ZEROES
* 76 - SENSE BYTES, NOT MONITOR BYTES TRANSFERRED
*
* 80 - UNEXPECTED STATUS ON SET INHIBIT
* 81 - UNEXPECTED INTERRUPT ON SET INHIBIT
* 82 - CC OF 3 ON SET INHIBIT
```

```
* 90 - UNEXPECTED STATUS ON RESET INHIBIT
* 91 - UNEXPECTED INTERRUPT ON RESET INHIBIT
* 92 - CC OF 3 ON RESET INHIBIT
*
* A0 - CC OF 1 ON SENSE
* A1 - STATUS NOT OC ON SENSE
* A2 - CC OF 3 ON SENSE
* A3 - INTERRUPT ADDRESS ERROR ON SENSE
* A4 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* A5 - INPUT SENSE BYTES ALL ZEROES
* A6 - SET INHIBIT BIT NOT CLEARED AFTER RESET INHIBIT COMMAND
*
* B0 - CC OF 0 ON SET SIMULATION MODE
* B1 - UNEXPECTED INTERRUPT ON SET SIMULATION MODE
* B2 - CC OF 3 ON SET SIMULATION MODE
* B3 - STATUS NOT OC ON SET SIMULATION MODE
*
* C0 - CC OF 1 ON SENSE
* C1 - STATUS NOT OC ON SENSE
* C2 - CC OF 3 ON SENSE
* C3 - INTERRUPT ADDRESS ERROR ON SENSE
* C4 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* C5 - INPUT SENSE BYTES ALL ZEROES
* C6 - FAULT FINDING MODE NOT SET AFTER SET SIMULATION MODE COMMAND
*
* D0 - CC OF 1 ON SIMULATED WRITE - U16/PHASE
* D1 - STATUS NOT OC ON SIMULATED WRITE
* D2 - CC OF 3 ON SIMULATED WRITE
* D3 - INTERRUPT ADDRESS ERROR ON SIMULATED WRITE
* D4 - FINAL BYTE COUNT ERROR ON SIMULATED WRITE (INITIAL VALUE = 4)
*
* E0 - CC OF 1 ON SENSE - U16/PHASE
* E1 - STATUS NOT OC ON SENSE
* E2 - CC OF 3 ON SENSE
* E3 - INTERRUPT ADDRESS ERROR ON SENSE
* E4 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* E5 - INPUT SENSE BYTES ALL ZEROES
* E6 - DT REGISTER NOT EQUAL TO EXPECTED VALUE
*
* F0 - CC OF 1 ON SIMULATED READ - U16/PHASE
* F1 - STATUS NOT OC ON SIMULATED READ
* F2 - CC OF 3 ON SIMULATED READ
* F3 - INPUT DATA FROM SIMULATED READ NOT EQUAL TO EXPECTED VALUE
*
* G0 - CC OF 1 ON SIMULATED WRITE - U12/PHASE
* G1 - STATUS NOT OC ON SIMULATED WRITE
* G2 - CC OF 3 ON SIMULATED WRITE
* G3 - INTERRUPT ADDRESS ERROR ON SIMULATED WRITE
* G4 - FINAL BYTE COUNT ERROR ON SIMULATED WRITE (INITIAL VALUE = 4)
*
```

```
* H0 - CC OF 1 ON SENSE - U12/PHASE
* H1 - STATUS NOT OC ON SENSE
* H2 - CC OF 3 ON SENSE
* H3 - INTERRUPT ADDRESS ERROR ON SENSE
* H4 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* H5 - INPUT SENSE BYTES ALL ZEROES
* H6 - DT REGISTER NOT EQUAL TO EXPECTED VALUE
*
* I0 - CC OF 1 ON SIMULATED READ - U12/PHASE
* I1 - STATUS NOT OC ON SIMULATED READ
* I2 - CC OF 3 ON SIMULATED READ
* I3 - INPUT DATA FROM SIMULATED READ NOT EQUAL TO EXPECTED VALUE
*
* J0 - CC OF 1 ON SIMULATED WRITE - U12/NRZI
* J1 - STATUS NOT OC ON SIMULATED WRITE
* J2 - CC OF 3 ON SIMULATED WRITE
* J3 - INTERRUPT ADDRESS ERROR ON SIMULATED WRITE
*
* K0 - CC OF 1 ON SENSE - U16/NRZI
* K1 - STATUS NOT OC ON SENSE
* K2 - CC OF 3 ON SENSE
* K3 - INTERRUPT ADDRESS ERROR ON SENSE
* K4 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* K5 - INPUT SENSE BYTES ALL ZEROES
* K6 - CRC REGISTER NOT EQUAL TO EXPECTED VALUE
*
* L0 - CC OF 1 ON SIMULATED READ - U16/NRZI
* L1 - STATUS NOT OC ON SIMULATED READ
* L2 - CC OF 3 ON SIMULATED READ
* L3 - INPUT DATA FROM SIMULATED READ NOT EQUAL TO EXPECTED VALUE
*
* M0 - CC OF 1 ON SIMULATED WRITE - U12/NRZI
* M1 - STATUS NOT OC ON SIMULATED WRITE
* M2 - CC OF 3 ON SIMULATED WRITE
* M3 - INTERRUPT ADDRESS ERROR ON SIMULATED WRITE
* M4 - FINAL BYTE COUNT ERROR ON SIMULATED WRITE (INITIAL VALUE = 4)
*
* N0 - CC OF 1 ON SENSE - U12/NRZI
* N1 - STATUS NOT OC ON SENSE
* N2 - CC OF 3 ON SENSE
* N3 - INTERRUPT ADDRESS ERROR ON SENSE
* N4 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* N5 - INPUT SENSE BYTES ALL ZEROES
* N6 - CRC REGISTER NOT EQUAL TO EXPECTED VALUE
*
* O0 - CC OF 1 ON SIMULATED READ - U12/NRZI
* O1 - STATUS NOT OC ON SIMULATED READ
* O2 - CC OF 3 ON SIMULATED READ
* O3 - INPUT DATA FROM SIMULATED READ NOT EQUAL TO EXPECTED VALUE
*
```

```
* P0 - CC OF 1 ON SIMULATED WRITE - U16/7-TK W/9-TK OPTION
* P1 - STATUS NOT OC ON SIMULATED WRITE
* P2 - CC OF 3 ON SIMULATED WRITE
* P3 - INTERRUPT ADDRESS ERROR ON SIMULATED WRITE
* P4 - FINAL BYTE COUNT ERROR ON SIMULATED WRITE (INITIAL VALUE = 4)
*
* Q0 - CC OF 1 ON SENSE - U16/7-TK W/9-TK OPTION
* Q1 - STATUS NOT OC ON SENSE
* Q2 - CC OF 3 ON SENSE
* Q3 - INTERRUPT ADDRESS ERROR ON SENSE
* Q4 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* Q5 - INPUT SENSE BYTES ALL ZEROES
* Q6 - CRC REGISTER NOT EQUAL TO EXPECTED VALUE
*
* R0 - CC OF 1 ON SIMULATED READ - U16/7-TK W/9-TK OPTION
* R1 - STATUS NOT OC ON SIMULATED READ
* R2 - CC OF 3 ON SIMULATED READ
* R3 - INPUT DATA FROM SIMULATED READ NOT EQUAL TO EXPECTED VALUE
*
* S0 - CC OF 1 ON SIMULATED WRITE - U16/7-TK W/9-TK OPTION
* S1 - STATUS NOT OC ON SIMULATED WRITE
* S2 - CC OF 3 ON SIMULATED WRITE
* S3 - INTERRUPT ADDRESS ERROR ON SIMULATED WRITE
* S4 - FINAL BYTE COUNT ERROR ON SIMULATED WRITE (INITIAL VALUE = 4)
*
* T0 - CC OF 1 ON SENSE - U16/7-TK W/9-TK OPTION
* T1 - STATUS NOT OC ON SENSE
* T2 - CC OF 3 ON SENSE
* T3 - INTERRUPT ADDRESS ERROR ON SENSE
* T4 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* T5 - INPUT SENSE BYTES ALL ZEROES
* T6 - CRC REGISTER NOT EQUAL TO EXPECTED VALUE
*
* U0 - UNEXPECTED STATUS ON DATA TRANSLATOR TURN-ON
* U1 - UNEXPECTED INTERRUPT ON DATA TRANSLATOR TURN ON
* U2 - CC OF 3 ON DATA TRANSLATOR TURN-ON
* U3 - BYTE COUNT ERROR ON DATA TRANSLATOR TURN-ON
*
* V0 - CC OF 1 ON SIMULATED READ - U16/7-TK W/9-TK OP DATA TRANS ON
* V1 - STATUS NOT OC ON SIMULATED READ
* V2 - CC OF 3 ON SIMULATED READ
* V3 - INPUT DATA FROM SIMULATED READ NOT EQUAL TO EXPECTED VALUE
*
* W0 - UNEXPECTED STATUS ON DATA TRANSLATOR TURN-OFF
* W1 - UNEXPECTED INTERRUPT ON DATA TRANSLATOR-OFF
* W2 - CC OF 3 ON DATA TRANSLATOR TURN-OFF
* W3 - BYTE COUNT ERROR ON DATA TRANSLATOR TURN-OFF
*
* X0 - CC OF 1 ON SIMULATED WRITE - U16/7-TK W/9-TK OPTION
* X1 - STATUS NOT OC ON SIMULATED WRITE
* X2 - CC OF 3 ON SIMULATED WRITE
* X3 - INTERRUPT ADDRESS ERROR ON SIMULATED WRITE
* X4 - FINAL BYTE COUNT ERROR ON SIMULATED WRITE (INITIAL VALUE = 4)
*
```

```
* Y0 - CC OF 1 ON SENSE - U16/7-TK W/9-TK OPTION
* Y1 - STATUS NOT OC ON SENSE
* Y2 - CC OF 3 ON SENSE
* Y3 - INTERRUPT ADDRESS ERROR ON SENSE
* Y4 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* Y5 - INPUT SENSE BYTES ALL ZEROES
* Y6 - CRC REGISTER NOT EQUAL TO EXPECTED VALUE
*
* Z0 - UNEXPECTED STATUS ON DATA CONVERTER TURN-ON
* Z1 - UNEXPECTED INTERRUPT ON DATA CONVERTER TURN-ON
* Z2 - CC OF 3 ON DATA CONVERTER TURN-ON
* Z3 - BYTE COUNT ERROR ON DATA CONVERTER TURN-ON
*
* 100 - CC OF 1 ON SIMULATED READ - U16/7-TK W/9-TK OP  DATA CONV ON
* 101 - STATUS NOT OC ON SIMULATED READ
* 102 - CC OF 3 ON SIMULATED READ
* 103 - INPUT DATA FROM SIMULATED READ NOT EQUAL TO EXPECTED VALUE
*
* 110 - UNEXPECTED STATUS ON DATA CONVERTER TURN-OFF
* 111 - UNEXPECTED INTERRUPT ON DATA CONVERTER TURN-OFF
* 112 - CC OF 3 ON DATA CONVERTER TURN-OFF
* 113 - BYTE COUNT ERROR ON DATA CONVERTER TURN-OFF
*
* 120 - CC OF 1 ON SIMULATED WRITE U12/7-TK W/9-TK OPTION
* 121 - STATUS NOT OC ON SIMULATED WRITE
* 122 - CC OF 3 ON SIMULATED WRITE
* 123 - INTERRUPT ADDRESS ERROR ON SIMULATED WRITE
* 124 - FINAL BYTE COUNT ERROR ON SIMULATED WRITE (INITIAL VALUE = 4)
*
* 130 - CC OF 1 ON SENSE - U12/7-TK W/9-TK OPTION
* 131 - STATUS NOT OC ON SENSE
* 132 - CC OF 3 ON SENSE
* 133 - INTERRUPT ADDRESS ERROR ON SENSE
* 134 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* 135 - INPUT SENSE BYTES ALL ZEROES
* 136 - CRC REGISTER NOT EQUAL TO EXPECTED VALUE
*
* 140 - CC OF 1 ON SIMULATED READ - U12/7-TK W/9-TK OPTION
* 141 - STATUS NOT OC ON SIMULATED READ
* 142 - CC OF 3 ON SIMULATED READ
* 143 - INPUT DATA FROM SIMULATED READ NOT EQUAL TO EXPECTED VALUE
*
* 150 - CC OF 1 ON SIMULATED WRITE U12/7-TK W/9-TK OPTION
* 151 - STATUS NOT OC ON SIMULATED WRITE
* 152 - CC OF 3 ON SIMULATED WRITE
* 153 - INTERRUPT ADDRESS ERROR ON SIMULATED WRITE
* 154 - FINAL BYTE COUNT ERROR ON SIMULATED WRITE (INITIAL VALUE = 4)
*
* 160 - CC OF 1 ON SENSE - U12/7-TK W/9-TK OPTION
* 161 - STATUS NOT OC ON SENSE
* 162 - CC OF 3 ON SENSE
* 163 - INTERRUPT ADDRESS ERROR ON SENSE
* 164 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
```

```
* 165 - INPUT SENSE BYTES ALL ZEROES
* 166 - CRC REGISTER NOT EQUAL TO EXPECTED VALUE
*
* 170 - UNEXPECTED STATUS ON DATA TRANSLATOR TURN-ON
* 171 - UNEXPECTED INTERRUPT ON DATA TRANSLATOR TURN-ON
* 172 - CC OF 3 ON DATA TRANSLATOR TURN-ON
* 173 - BYTE COUNT ERROR ON DATA TRANSLATOR TURN-ON
*
* 180 - CC OF 1 ON SIMULATED READ - U12/7-TK W/9-TK OP DATA TRANS ON
* 181 - STATUS NOT OC ON SIMULATED READ
* 182 - CC OF 3 ON SIMULATED READ
* 183 - INPUT DATA FROM SIMULATED READ NOT EQUAL TO EXPECTED VALUE
*
* 190 - UNEXPECTED STATUS ON DATA TRANSLATOR TURN-OFF
* 191 - UNEXPECTED INTERRUPT ON DATA TRANSLATOR TURN-OFF
* 192 - CC OF 3 ON DATA TRANSLATOR TURN-OFF
* 193 - BYTE COUNT ERROR ON DATA TRANSLATOR TURN-OFF
*
* 1A0 - CC OF 1 ON SIMULATED WRITE U12/7-TK W/9-TK OPTION
* 1A1 - STATUS NOT OC ON SIMULATED WRITE
* 1A2 - CC OF 3 ON SIMULATED WRITE
* 1A3 - INTERRUPT ADDRESS ERROR ON SIMULATED WRITE
* 1A4 - FINAL BYTE COUNT ERROR ON SIMULATED WRITE (INITIAL VALUE = 4)
*
* 1B0 - CC OF 1 ON SENSE - U12/7-TK W/9-TK OPTION
* 1B1 - STATUS NOT OC ON SENSE
* 1B2 - CC OF 3 ON SENSE
* 1B3 - INTERRUPT ADDRESS ERROR ON SENSE
* 1B4 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* 1B5 - INPUT SENSE BYTES ALL ZEROES
* 1B6 - CRC REGISTER NOT EQUAL TO EXPECTED VALUE
*
* 1C0 - UNEXPECTED STATUS ON DATA CONVERTER TURN-ON
* 1C1 - UNEXPECTED INTERRUPT ON DATA CONVERTER TURN-ON
* 1C2 - CC OF 3 ON DATA CONVERTER TURN-ON
* 1C3 - BYTE COUNT ERROR ON DATA CONVERTER TURN-ON
*
* 1D0 - CC OF 1 ON SIMULATED READ - U12/7-TK W/9-TK OP DATA CONV ON
* 1D1 - STATUS NOT OC ON SIMULATED READ
* 1D2 - CC OF 3 ON SIMULATED READ
* 1D3 - INPUT DATA FROM SIMULATED READ NOT EQUAL TO EXPECTED VALUE
*
* 1E0 - UNEXPECTED STATUS ON DATA CONVERTER TURN-OFF
* 1E1 - UNEXPECTED INTERRUPT ON DATA CONVERTER TURN-OFF
* 1E2 - CC OF 3 ON DATA CONVERTER TURN-OFF
* 1E3 - BYTE COUNT ERROR ON DATA CONVERTER TURN-OFF
*
* 1F0 - CC OF 1 ON SIMULATED WRITE - U16/7-TRACK
* 1F1 - STATUS NOT OC ON SIMULATED WRITE
* 1F2 - CC OF 3 ON SIMULATED WRITE
* 1F3 - INTERRUPT ADDRESS ERROR ON SIMULATED WRITE
* 1F4 - FINAL BYTE COUNT ERROR ON SIMULATED WRITE (INITIAL VALUE = 4)
*
```

```
* 1G0 - CC OF 1 ON SENSE - U16/7-TRACK
* 1G1 - STATUS NOT OC ON SENSE
* 1G2 - CC OF 3 ON SENSE
* 1G3 - INTERRUPT ADDRESS ERROR ON SENSE
* 1G4 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* 1G5 - INPUT SENSE BYTES ALL ZEROES
* 1G6 - CRC REGISTER NOT EQUAL TO EXPECTED VALUE
*
* 1H0 - CC OF 1 ON SIMULATED READ - U16/7-TRACK
* 1H1 - STATUS NOT OC ON SIMULATED READ
* 1H2 - CC OF 3 ON SIMULATED READ
* 1H3 - INPUT DATA FROM SIMULATED READ NOT EQUAL TO EXPECTED VALUE
*
* 1I0 - CC OF 1 ON SIMULATED WRITE - U16/7-TRACK
* 1I1 - STATUS NOT OC ON SIMULATED WRITE
* 1I2 - CC OF 3 ON SIMULATED WRITE
* 1I3 - INTERRUPT ADDRESS ERROR ON SIMULATED WRITE
* 1I4 - FINAL BYTE COUNT ERROR ON SIMULATED WRITE (INITIAL VALUE = 4)
*
* 1J0 - CC OF 1 ON SENSE - U16/7-TRACK
* 1J1 - STATUS NOT OC ON SENSE
* 1J2 - CC OF 3 ON SENSE
* 1J3 - INTERRUPT ADDRESS ERROR ON SENSE
* 1J4 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* 1J5 - INPUT SENSE BYTES ALL ZEROES
* 1J6 - CRC REGISTER NOT EQUAL TO EXPECTED VALUE
*
* 1K0 - UNEXPECTED STATUS ON DATA TRANSLATOR TURN-ON
* 1K1 - UNEXPECTED INTERRUPT ON DATA TRANSLATOR TURN-ON
* 1K2 - CC OF 3 ON DATA TRANSLATOR TURN-ON
* 1K3 - BYTE COUNT ERROR ON DATA TRANSLATOR TURN-ON
*
* 1L0 - CC OF 1 ON SIMULATED READ - U16/7-TRACK
* 1L1 - STATUS NOT OC ON SIMULATED READ
* 1L2 - CC OF 3 ON SIMULATED READ
* 1L3 - INPUT DATA FROM SIMULATED READ NOT EQUAL TO EXPECTED VALUE
*
* 1M0 - UNEXPECTED STATUS ON DATA TRANSLATOR TURN-OFF
* 1M1 - UNEXPECTED INTERRUPT ON DATA TRANSLATOR TURN-OFF
* 1M2 - CC OF 3 ON DATA TRANSLATOR TURN-OFF
* 1M3 - BYTE COUNT ERROR ON DATA TRANSLATOR TURN-OFF
*
* 1N0 - CC OF 1 ON SIMULATED WRITE - U16/7-TRACK
* 1N1 - STATUS NOT OC ON SIMULATED WRITE
* 1N2 - CC OF 3 ON SIMULATED WRITE
* 1N3 - INTERRUPT ADDRESS ERROR ON SIMULATED WRITE
* 1N4 - FINAL BYTE COUNT ERROR ON SIMULATED WRITE (INITIAL VALUE = 4)
*
* 100 - CC OF 1 ON SENSE - U16/7-TRACK
* 101 - STATUS NOT OC ON SENSE
* 102 - CC OF 3 ON SENSE
* 103 - INTERRUPT ADDRESS ERROR ON SENSE
```

```
* 1O4 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* 1O5 - INPUT SENSE BYTES ALL ZEROES
* 1O6 - CRC REGISTER NOT EQUAL TO EXPECTED VALUE
*
* 1PO - UNEXPECTED STATUS ON DATA CONVERTER TURN-ON
* 1P1 - UNEXPECTED INTERRUPT ON DATA CONVERTER TURN-ON
* 1P2 - CC OF 3 ON DATA CONVERTER TURN-ON
* 1P3 - BYTE COUNT ERROR ON DATA CONVERTER TURN-ON
*
* 1QO - CC OF 1 ON SIMULATED READ - U16/7-TRACK
* 1Q1 - STATUS NOT OC ON SIMULATED READ
* 1Q2 - CC OF 3 ON SIMULATED READ
* 1Q3 - INPUT DATA FROM SIMULATED READ NOT EQUAL TO EXPECTED VALUE
*
* 1RO - UNEXPECTED STATUS ON DATA CONVERTER TURN-OFF
* 1R1 - UNEXPECTED INTERRUPT ON DATA CONVERTER TURN-OFF
* 1R2 - CC OF 3 ON DATA CONVERTER TURN-OFF
* 1R3 - BYTE COUNT ERROR ON DATA CONVERTER TURN-OFF
*
* 1SO - CC OF 1 ON SIMULATED WRITE - U12/7-TRACK
* 1S1 - STATUS NOT OC ON SIMULATED WRITE
* 1S2 - CC OF 3 ON SIMULATED WRITE
* 1S3 - INTERRUPT ADDRESS ERROR ON SIMULATED WRITE
* 1S4 - FINAL BYTE COUNT ERROR ON SIMULATED WRITE (INITIAL VALUE = 4)
*
* 1TO - CC OF 1 ON SENSE - U12/7-TRACK
* 1T1 - STATUS NOT OC ON SENSE
* 1T2 - CC OF 3 ON SENSE
* 1T3 - INTERRUPT ADDRESS ERROR ON SENSE
* 1T4 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* 1T5 - INPUT SENSE BYTES ALL ZEROES
* 1T6 - CRC REGISTER NOT EQUAL TO EXPECTED VALUE
*
* 1UO - CC OF 1 ON SIMULATED READ - U12/7-TRACK
* 1U1 - STATUS NOT OC ON SIMULATED READ
* 1U2 - CC OF 3 ON SIMULATED READ
* 1U3 - INPUT DATA FROM SIMULATED READ NOT EQUAL TO EXPECTED VALUE
*
* 1VO - CC OF 1 ON SIMULATED WRITE - U12/7-TRACK
* 1V1 - STATUS NOT OC ON SIMULATED WRITE
* 1V2 - CC OF 3 ON SIMULATED WRITE
* 1V3 - INTERRUPT ADDRESS ERROR ON SIMULATED WRITE
* 1V4 - FINAL BYTE COUNT ERROR ON SIMULATED WRITE (INITIAL VALUE = 4)
*
* 1WO - CC OF 1 ON SENSE - U12/7-TRACK
* 1W1 - STATUS NOT OC ON SENSE
* 1W2 - CC OF 3 ON SENSE
* 1W3 - INTERRUPT ADDRESS ERROR ON SENSE
* 1W4 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* 1W5 - INPUT SENSE BYTES ALL ZEROES
* 1W6 - CRC REGISTER NOT EQUAL TO EXPECTED VALUE
*
```

```
* 1X0 - UNEXPECTED STATUS ON DATA TRANSLATOR TURN-ON
* 1X1 - UNEXPECTED INTERRUPT ON DATA TRANSLATOR TURN-ON
* 1X2 - CC OF 3 ON DATA TRANSLATOR TURN-ON
* 1X3 - BYTE COUNT ERROR ON DATA TRANSLATOR TURN-ON
*
* 1Y0 - CC OF 1 ON SIMULATED READ - U12/7-TRACK
* 1Y1 - STATUS NOT OC ON SIMULATED READ
* 1Y2 - CC OF 3 ON SIMULATED READ
* 1Y3 - INPUT DATA FROM SIMULATED READ NOT EQUAL TO EXPECTED VALUE
*
* 1Z0 - UNEXPECTED STATUS ON DATA TRANSLATOR TURN-OFF
* 1Z1 - UNEXPECTED INTERRUPT ON DATA TRANSLATOR TURN-OFF
* 1Z2 - CC OF 3 ON DATA TRANSLATOR TURN-OFF
* 1Z3 - BYTE COUNT ERROR ON DATA TRANSLATOR TURN-OFF
*
* 210 - CC OF 1 ON SIMULATED WRITE - U12/7-TRACK
* 211 - STATUS NOT OC ON SIMULATED WRITE
* 212 - CC OF 3 ON SIMULATED WRITE
* 213 - INTERRUPT ADDRESS ERROR ON SIMULATED WRITE
* 214 - FINAL BYTE COUNT ERROR ON SIMULATED WRITE (INITIAL VALUE = 4)
*
* 220 - CC OF 1 ON SENSE - U12/7-TRACK
* 221 - STATUS NOT OC ON SENSE
* 222 - CC OF 3 ON SENSE
* 223 - INTERRUPT ADDRESS ERROR ON SENSE
* 224 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* 225 - INPUT SENSE BYTES ALL ZEROES
* 226 - CRC REGISTER NOT EQUAL TO EXPECTED VALUE
*
* 230 - UNEXPECTED STATUS ON DATA CONVERTER TURN-ON
* 231 - UNEXPECTED INTERRUPT ON DATA CONVERTER TURN-ON
* 232 - CC OF 3 ON DATA CONVERTER TURN-ON
* 233 - BYTE COUNT ERROR ON DATA CONVERTER TURN-ON
*
* 240 - CC OF 1 ON SIMULATED READ - U12/7-TRACK
* 241 - STATUS NOT OC ON SIMULATED READ
* 242 - CC OF 3 ON SIMULATED READ
* 243 - INPUT DATA FROM SIMULATED READ NOT EQUAL TO EXPECTED VALUE
*
* 250 - UNEXPECTED STATUS ON DATA CONVERTER TURN-OFF
* 251 - UNEXPECTED INTERRUPT ON DATA CONVERTER TURN-OFF
* 252 - CC OF 3 ON DATA CONVERTER TURN-OFF
* 253 - BYTE COUNT ERROR ON DATA CONVERTER TURN-OFF
*
* 260 - CC OF 0 ON RESET FAULT-FINDING MODE
* 261 - UNEXPECTED INTERRUPT ON RESET FAULT-FINDING MODE
* 262 - CC OF 3 ON RESET FAULT-FINDING MODE
* 263 - STATUS NOT OC ON RESET FAULT-FINDING MODE
*
* 270 - CC OF 1 ON SENSE
* 271 - STATUS NOT OC ON SENSE
* 272 - CC OF 3 ON SENSE
* 273 - INTERRUPT ADDRESS ERROR ON SENSE
```

```
* 274 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* 275 - INPUT SENSE BYTES ALL ZEROES
* 276 - MONITOR BYTES, NOT SENSE BYTES TRANSFERRED
*
* 280 - CC OF 0 ON SET MONITOR MODE
* 281 - UNEXPECTED INTERRUPT ON SET MONITOR MODE
* 282 - CC OF 3 ON SET MONITOR MODE
* 283 - STATUS NOT OC ON SET MONITOR MODE
*
* 290 - CC OF 1 ON SENSE
* 291 - STATUS NOT OC ON SENSE
* 292 - CC OF 3 ON SENSE
* 293 - INTERRUPT ADDRESS ERROR ON SENSE
* 294 - FINAL BYTE COUNT ERROR ON SENSE (INITIAL VALUE = 5)
* 295 - INPUT SENSE BYTES ALL ZEROES
* 296 - SENSE BYTES, NOT MONITOR BYTES TRANSFERRED
*
* 2A0 - CC OF 1 ON SENSE/RESERVE
* 2A1 - STATUS NOT OC ON SENSE/RESERVE
* 2A2 - CC OF 3 ON SENSE/RESERVE
* 2A3 - INTERRUPT ADDRESS ERROR ON SENSE/RESERVE
* 2A4 - FINAL BYTE COUNT ERROR ON S/R (INITIAL VALUE = 5)
* 2A5 - INPUT SENSE BYTES ALL ZEROES
* 2A6 - CHANNEL INTERFACE NOT RESERVED AFTER SENSE/RESERVE COMMAND
*
* 2B0 - CC OF 0 ON SENSE
* 2B1 - CC OF 3 ON SENSE
* 2B2 - CONTROL UNIT NOT BUSY AFTER SNS/RSV ON 1ST CHANNEL
*
* 2C0 - CC OF 1 ON SENSE RELEASE
* 2C1 - STATUS NOT OC ON SENSE/RELEASE
* 2C2 - CC OF 3 ON SENSE/RELEASE
* 2C3 - INTERRUPT ADDRESS ERROR ON SENSE/RELEASE
* 2C4 - FINAL BYTE COUNT ERROR ON SENSE/RELEASE (INITIAL VALUE = 5)
* 2C5 - INPUT SENSE BYTES ALL ZEROES
* 2C6 - CHN INTFC NOT RELEASED AFTER SENSE/RELEASE COMMAND
*
* 2D0 - CC OF 1 ON SENSE/RESERVE
* 2D1 - STATUS NOT OC ON SENSE/RESERVE
* 2D2 - CC OF 3 ON SENSE/RESERVE
* 2D3 - INTERRUPT ADDRESS ERROR ON SENSE/RESERVE
* 2D4 - FINAL BYTE COUNT ERROR ON S/R (INITIAL VALUE = 5)
* 2D5 - INPUT SENSE BYTES ALL ZEROES
* 2D6 - CHANNEL INTERFACE NOT RESERVED AFTER SENSE/RESERVE COMMAND
*
* 2E0 - CC OF 0 ON SENSE
* 2E1 - CC OF 3 ON SENSE
* 2E2 - CONTROL UNIT NOT BUSY AFTER SENSE/RESERVE ON 2ND CHANNEL
*
* 2F0 - CC OF 1 ON SENSE/RELEASE
* 2F1 - STATUS NOT OC ON SENSE/RELEASE
* 2F2 - CC OF 3 ON SENSE/RELEASE
* 2F3 - INTERRUPT ADDRESS ERROR ON SENSE/RELEASE
```

```
* 2F4 - FINAL BYTE COUNT ERROR ON SENSE/RELEASE (INITIAL VALUE = 5)
* 2F5 - INPUT SENSE BYTES ALL ZEROES
* 2F6 - CHN INTFC NOT RELEASED AFTER SENSE/RELEASE COMMAND
*
* 2I0 - CC OF 1 ON WRITE (PRI. CHN)
* 2I1 - CC OF 3 ON WRITE (PRI. CHN)
* 2I2 - STATUS NOT OC ON WRITE (PRI CHN)
* 2I3 - RESIDUAL BYTE COUNT NOT = 0 AFTER WRITE (PRI. CHN)
*
* 2J0 - CC OF 1 ON WRITE (SEC. CHN) OR READ BKWD (PRI. CHN)
* 2J1 - CC OF 3 ON WRITE (SEC. CHN) OR READ BKWD (PRI. CHN)
* 2J2 - STATUS NOT OC ON CHN 1
* 2J3 - STATUS NOT OC ON CHN 2
* 2J4 - RESIDUAL BYTE COUNT NOT = 0 ON CHN 1
* 2J5 - RESIDUAL BYTE COUNT NOT = 0 ON CHN 2
*
* 2G0 - CC = 0 ON ERASE (CHN 1) OR ERASE (CHN 2)
* 2G1 - CC = 3 ON ERASE (CHN 1) OR ERASE (CHN 2)
* 2G2 - BAD STATUS ON ERASE (CHN 1)
* 2G3 - BAD STATUS ON ERASE (CHN 2)
* 2G4 - RESIDUAL BYTE COUNT NOT = 0 ON CHN 1
* 2G5 - RESIDUAL BYTE COUNT NOT = 0 ON CHN 2
*
* 2K0 - CC OF 1 ON WRITE (PRI. CHN) OR READ BKWD (SEC. CHN)
* 2K1 - CC OF 3 ON WRITE (PRI. CHN) OR READ BKWD (SEC. CHN)
* 2K2 - STATUS NOT OC ON CHN 1
* 2K3 - STATUS NOT OC ON CHN 2
* 2K4 - RESIDUAL BYTE COUNT NOT = 0 ON CHN 1
* 2K5 - RESIDUAL BYTE COUNT NOT = 0 ON CHN 2
*
* 2L0 - CC OF 1 ON READ BKWD (PRI. CHN) OR READ (SEC. CHN)
* 2L1 - CC OF 3 ON READ BKWD (PRI. CHN) OR READ (SEC. CHN)
* 2L2 - STATUS NOT OC ON CHN 1
* 2K3 - STATUS NOT OC ON CHN 2
* 2L4 - RESIDUAL BYTE COUNT NOT = 0 ON CHN 1
* 2L5 = RESIDUAL BYTE COUNT NOT = 0 ON CHN 2
*
* 2M0 - CC OF 1 ON WRITE (CHN 1) OR WRITE (CHN 2)
* 2M1 - CC OF 3 ON WRITE (CHN 1) OR WRITE (CHN 2)
* 2M2 - STATUS NOT OC ON WRITE (CHN 1)
* 2M3 - STATUS NOT OC ON WRITE (CHN 2)
* 2M4 - RESIDUAL BYTE COUNT NOT = 0 AFTER WRITE (CHN 1)
* 2M5 = RESIDUAL BYTE COUNT NOT = 0 AFTER WRITE (CHN 2)
*
*****************************************************************************************
```

4. SUPPLEMENTARY DATA

4.1 Simulate Mode Data Patterns (4-Byte Data Transfer)

4.1.1 Simulated Writes - 4-Byte Output For all Simulated Writes: $BCEA8F3E_{16}$

4.1.2 9 - Track Phase Mode -

A. CRC Register after Simulated Write: $ØØ_{16}$ = $ØØØØØØØØØ_2$ (even parity)

B. Input data after Simulated Read: $00FF00FF_{16}$

4.1.3 9 - Track NRZI Mode -

A. CRC Register after Simulated Write: $B4_{16}$ =010110100_2 (even parity)

B. Input data after Simulated Read: $638DFAC1_{16}$

4.1.4 7 - Track if 9 - Track NRZI Present -

A. CRC Register after Simulated Write: 39_{16} = $ØØØ111ØØ1_2$ (even parity)

B. Input data after Simulated Read: $3B321624_{16}$

C. Input data after Simlulated Read with Data Translater on: $4BC2E6D4_{16}$

D. Input data after Simulated Read with Data Converter on: $EF25A4F5_{16}$

4.1.5 7 - Track if 9 - Track NRZI Not Present -

A. CRC Register after Simulated Write: $3F_{16}$ = 100111111_2 (odd parity)

B. Input data after Simulated Read: $3F3F3F3F_{16}$

C. Input data after Simulated Read with Data Translator on: $4F4F4F4F_{16}$

D. Input data after Simulated Read with Data Converter on: $FFFFFFFF_{16}$

4.2 Derivation of CRC Register and Input Data (Simulate Mode)

4.2.1 9-Track Phase - Hardwired -

A, CRC = ØØ

B. Input = ØØFFØØFF...

4.2.2 9-Track NRZI -

A. CRC Register

PØ1234567	
Ø1Ø1111ØØ	1st data byte
ØØØØØØØØØ	Initial CRC Register
Ø1Ø1111ØØ	Exclusive OR
ØØ1Ø1111Ø	Right Circular Shift 1 bit
ØØØØØØØØØ	feedback bits
ØØ1Ø1111Ø	Exclusive OR
Ø111Ø1Ø1Ø	2nd data byte
Ø1Ø11Ø1ØØ	Exclusive OR
ØØ1Ø11Ø1Ø	Right Circular Shift 1 bit
ØØØØØØØØØ	feedback bits
ØØ1Ø11Ø1Ø	Exclusive OR
Ø1ØØØ1111	3rd data byte
Ø11Ø1Ø1Ø1	Exclusive OR
1Ø11Ø1Ø1Ø	Right Circular Shift 1 bit
ØØØ1111ØØ	feedback bits
1Ø1Ø1Ø11Ø	Exclusive OR
ØØØ11111Ø	4th data byte
1Ø11Ø1ØØØ	Exclusive OR
Ø1Ø11Ø1ØØ	Right Circular Shift 1 bit
ØØØØØØØØØ	feedback Bits
Ø1Ø11Ø1ØØ	Exclusive OR

Final CRC Character
$B4_{16}$

B. Input Data

PØ1234567	
Ø1Ø11Ø1ØØ	initial CRC Register (from previous Simulated Write)
111Ø1Ø111	Read out Pattern (D7)

ØØØ111ØØ1	Right Circular Shift 1 bit
ØØØØØØØØØ	feedback bits
ØØØ111ØØ1	Exclusive OR

Final CRC Register Character

39_{16}

B. Input Data

PØ1234567

ØØØ111ØØ1	initial CRC Register
111Ø1Ø111	Read out Pattern (D7)
1111Ø111Ø	Exclusive OR (1st data byte) = $3B_{16}$
1ØØØ111ØØ	Right Circular Shift CRC Register 1 bit
111Ø1Ø111	Read out Pattern (D7)
Ø11ØØ1Ø11	Exclusive OR (2nd data byte) = 32_{16}
Ø1ØØØ111Ø	Right Circular Shift CRC Register 1 bit
111Ø1Ø111	Read out Pattern (D7)
1Ø1Ø11ØØ1	Exclusive OR (3rd data byte) = 16_{16}
ØØ1ØØØ111	Right Circular Shift CRC Register 1 bit
111Ø1Ø111	Read out Pattern (D7)
11ØØ1ØØØØ	Exclusive OR (4th data byte) = 24_{16}

Data Translator and Data Converter results are derived in the normal fashion. The above data bytes are used as input.

4.2.4 7-Track with 9-Track NRZI Not Present -

A. CRC Register is hardwired = $3F_{16}$ ($1ØØ111111_2$)

B. Input data is hardwired = 3F3F3F3F...

Data Translator and Data Converter results are derived in the normal fashion. The above data bytes are used as input.

4.3 Figure 1 - The following table lists and describes the simulated devices to which this test issues commands.

SIMULATED SERVO SELECTION

Device Address (Unit Register)				Servo Type	Head Type	Recording Capability	
4	5	6	7				
0	0	0	0	XVI	9-Track	Phase	Basic Unit
0	0	0	1	XII	9-Track	Phase	
0	0	1	0	XVI	9-Track	NRZI	
0	0	1	1	XII	9-Track		
0	1	0	0	XVI	7-Track		
0	1	0	1	XII	7-Track	NRZI	